In the Claims

Please remove claims 1 to 45 from prosecution as they have been allowed and will issue in the parent application.

Please add the following new claims 46 to 91:

46. A high f_{MAX} deep submicron MOSFET structure, comprising:

a substrate;

a MOSFET on the substrate; the MOSFET having a source and a drain and including a silicide portion over a gate electrode;

a first ILD layer over the substrate and the MOSFET wherein the silicide portion over the gate electrode is exposed;

a metal gate portion:

over the first ILD layer; and

over the silicide portion over the gate electrode;

the metal gate portion having a width substantially greater than the width of the silicide portion over the gate electrode;

a second ILD layer over the metal gate portion and the first ILD layer;

a first metal contact through the second ILD layer contacting the metal gate portion; and

a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high f_{MAX} deep submicron MOSFET structure;

whereby the width of the metal gate portion reduces R_g and increases the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

47. The structure of claim 46, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

under the first ILD layer.

48. The structure of claim 46, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

between the first ILD layer;

the dielectric layer being comprised of Si_3N_4 or SiON.

49. The structure of claim 46, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised of $CoSi_x$, $CoSi_2$, or $TiSi_2$; the first ILD layer is comprised of oxide, silicon oxide, USG or TEOS; the metal gate portion is comprised of W, Al, Cu, TiN or Au; the second ILD layer is comprised of

oxide, silicon oxide, HDP or FSG; and the first and second metal contacts are each comprised of W or Cu.

50. The structure of claim 46, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised $CoSi_x$; the first ILD layer is comprised of silicon oxide; the metal gate portion is comprised of tungsten; the second ILD layer is comprised silicon oxide; and the first and second metal contacts each being comprised of tungsten.

51. The structure of claim 46, wherein the gate electrode has a width of from about 500 to 5000Å and the metal gate portion has a width of from about 500 to 8000Å.

52. The structure of claim 46, wherein the gate electrode has a width of from about 1000 to 3500Å and the metal gate portion has a width of from about 1000 to 3000Å.

53. The structure of claim 46, wherein the gate electrode has a width of about 0.13μm and the metal gate portion has a width of from about 1800 to 2400Å.

54. The structure of claim 46, wherein the gate electrode has a height of from about 1000 to 3000Å; the silicide portion over the gate electrode has a thickness of from

about 270 to 330Å; the first ILD layer has a thickness of from about 1700 to 1900Å; and the metal gate portion has a thickness of from about 1800 to 2200Å.

55. The structure of claim 46, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of from about 290 to 310Å; the first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of from about 1900 to 2100Å.

56. The structure of claim 46, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of about 300Å; the first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of about 2000Å.

57. The structure of claim 46, wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain silicide portion.

58. The structure of claim 46, wherein the MOSFET includes a source $CoSi_x$ silicide portion over at least a portion of the source and a drain $CoSi_x$ silicide portion over

at least a portion of the drain; and wherein the second metal contact contacts the drain $CoSi_x$ silicide portion.

59. The structure of claim 46, wherein the first ILD layer is planarized.

60. The structure of claim 46, wherein the high f_{MAX} deep submicron MOSFET structure is positioned within an RF circuit.

61. The structure of claim 46, wherein the gate electrode has a gate oxide thereunder; the gate oxide having a thickness proximate the source and drain to significantly reduce the parasitic capacitance and increase the f_{max} of the high f_{MAX} deep submicron MOSFET structure.

62. A high f_{MAX} deep submicron MOSFET structure, comprising:

a substrate;

a MOSFET on the substrate; the MOSFET having a source and a drain and including a silicide portion over a gate electrode; the gate electrode having a width of from about 500 to 5000Å;

a first ILD layer over the substrate and the MOSFET wherein the silicide portion over the gate electrode is exposed;

a metal gate portion:

over the first ILD layer;

and over the silicide portion over the gate electrode;

the metal gate portion having a width of from about 500 to 8000Å;

a second ILD layer over the metal gate portion and the first ILD layer;

a first metal contact through the second ILD layer contacting the metal gate portion; and

a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high f_{MAX} deep submicron MOSFET structure;

whereby the width of the metal gate portion reduces R_g and increases the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

63. The structure of claim 62, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

under the first ILD layer.

64. The structure of claim 62, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

between the first ILD layer;

the dielectric layer being comprised of Si_3N_4 or SiON.

65. The structure of claim 62, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised of $CoSi_x$, $CoSi_2$ or $TiSi_2$; the first ILD layer is comprised of oxide, silicon oxide, USG or TEOS; the metal gate portion is comprised of W, Al, Cu, TiN or Au; the second ILD layer is comprised of oxide, silicon oxide, HDP or FSG; and the first and second metal contacts are each comprised of W or Cu.

66. The structure of claim 62, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised $CoSi_x$; the first ILD layer is comprised of silicon oxide; the metal gate portion is comprised of tungsten; the

second ILD layer is comprised silicon oxide; and the first and second metal contacts each being comprised of tungsten.

67. The structure of claim 62, wherein the gate electrode has a width of from about 1000 to 3500Å and the metal gate portion has a width of from about 1000 to 3000Å.

68. The structure of claim 62, wherein the gate electrode has a width of about 0.13μm and the metal gate portion has a width of from about 1800 to 2400Å.

69. The structure of claim 62, wherein the gate electrode has a height of from about 1000 to 3000Å; the silicide portion over the gate electrode has a thickness of from about 270 to 330Å; the first ILD layer has a thickness of from about 1700 to 1900Å; and the metal gate portion has a thickness of from about 1800 to 2200Å

70. The structure of claim 62, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of from about 290 to 310Å; the first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of from about 1900 to 2100Å.

71. The structure of claim 62, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion 30 over the gate electrode 18 has a thickness of

about 300Å; the first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of about 2000Å.

72. The structure of claim 62, wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain silicide portion.

73. The structure of claim 62, wherein the MOSFET includes a source $CoSi_x$ silicide portion over at least a portion of the source and a drain $CoSi_x$ silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain $CoSi_x$ silicide portion.

74. The structure of claim 62, wherein the high f_{MAX} deep submicron MOSFET structure is positioned within an RF circuit.

75. The structure of claim 62, wherein the gate electrode has a gate oxide thereunder; the gate oxide having a thickness proximate the source and drain to significantly reduce the parasitic capacitance and increase the f_{max} of the high f_{MAX} deep submicron MOSFET structure.

76. The structure of claim 62, wherein the first ILD layer is planarized.

77. A high f_{MAX} deep submicron MOSFET structure, comprising:

a substrate;

a MOSFET on the substrate; the MOSFET having a source and a drain and including a silicide portion over a gate electrode; the gate electrode having a gate oxide thereunder; the gate oxide having a thickness proximate the source and drain to significantly reduce the parasitic capacitance and increase the f_{max} of the high f_{MAX} deep submicron MOSFET structure;

a first ILD layer over the substrate and the MOSFET wherein the silicide portion over the gate electrode is exposed;

a metal gate portion:

over the first ILD layer; and

over the silicide portion over the gate electrode;

the metal gate portion having a width substantially greater than the width of the silicide portion over the gate electrode;

a second ILD layer over the metal gate portion and the first ILD layer;

a first metal contact through the second ILD layer contacting the metal gate portion; and

a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high f_{MAX} deep submicron MOSFET structure;

whereby the width of the metal gate portion reduces R_g and increases the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

78. The structure of claim 77, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

under the first ILD layer.

79. The structure of claim 77, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

between the first ILD layer;

the dielectric layer being comprised of Si_3N_4 or SiON.

80. The structure of claim 77, wherein the gate electrode is comprised polysilicon; the silicide portion over the gate electrode is comprised of $CoSi_x$, $CoSi_2$, or $TiSi_2$; the first ILD layer is comprised of oxide, silicon oxide, USG or TEOS; the metal gate portion is comprised of W, Al, Cu, TiN or Au; the second ILD layer is comprised of

oxide, silicon oxide, HDP or FSG; and the first and second metal contacts are each comprised of W or Cu.

81. The structure of claim 77, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised of $CoSi_x$; the first ILD layer is comprised of silicon oxide; the metal gate portion is comprised of tungsten; the second ILD layer is comprised of silicon oxide; and the first and second metal contacts are each comprised of tungsten.

82. The structure of claim 77, wherein the gate electrode has a width of from about 500 to 5000Å and the metal gate portion has a width of from about 500 to 8000Å.

83. The structure of claim 77, wherein the gate electrode has a width of from about 1000 to 3500Å and the metal gate portion has a width of from about 1000 to 3000Å.

84. The structure of claim 77, wherein the gate electrode has a width of about 0.13μm and the metal gate portion has a width of from about 1800 to 2400Å.

85. The structure of claim 77, wherein the gate electrode has a height of from about 1000 to 3000Å; the silicide portion over the gate electrode has a thickness of from

about 270 to 330Å; the first ILD layer has a thickness of from about 1700 to 1900Å; and the metal gate portion has a thickness of from about 1800 to 2200Å.

86. The structure of claim 77, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of from about 290 to 310Å; the first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of from about 1900 to 2100Å.

87. The structure of claim 77, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of about 300Å; the first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of about 2000Å.

88. The structure of claim 77, wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain silicide portion.

89. The structure of claim 77, wherein the MOSFET includes a source $CoSi_x$ silicide portion over at least a portion of the source and a drain $CoSi_x$ silicide portion over

at least a portion of the drain; and wherein the second metal contact contacts the drain $CoSi_x$ silicide portion.

90. The structure of claim 77, wherein the first ILD layer is planarized.

91. The structure of claim 77, wherein the high f_{MAX} deep submicron MOSFET structure is positioned within an RF circuit.

Remarks

In the Claims

Claims 1 to 45 have been removed from prosecution as they have been allowed and will issue in the parent application.

Claims 46 to 91 are new and have been added to better encompass the full scope and breadth of the invention notwithstanding the patentability of the original claims.

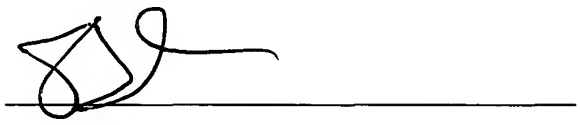
CONCLUSION

Allowance of all claims is requested. Issuance of the application is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

It is requested that the Examiner issue only written Office Actions and communications in this application.

Respectively submitted,



Stephen B. Ackerman

Reg. No. 37,761

Version with markings to show changes made.

Please add the following claims:

-- 46. A high f_{MAX} deep submicron MOSFET structure, comprising:

a substrate;

a MOSFET on the substrate; the MOSFET having a source and a drain and including a silicide portion over a gate electrode;

a first ILD layer over the substrate and the MOSFET wherein the silicide portion over the gate electrode is exposed;

a metal gate portion:

over the first ILD layer; and

over the silicide portion over the gate electrode;

the metal gate portion having a width substantially greater than the width of the silicide portion over the gate electrode;

a second ILD layer over the metal gate portion and the first ILD layer;

a first metal contact through the second ILD layer contacting the metal gate portion; and

a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high f_{MAX} deep submicron MOSFET structure;

whereby the width of the metal gate portion reduces R_g and increases the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

47. The structure of claim 46, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

under the first ILD layer.

48. The structure of claim 46, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

between the first ILD layer;

the dielectric layer being comprised of Si_3N_4 or SiON.

49. The structure of claim 46, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised of $CoSi_x$, $CoSi_2$, or $TiSi_2$; the first ILD layer is comprised of oxide, silicon oxide, USG or TEOS; the metal gate portion is comprised of W, Al, Cu, TiN or Au; the second ILD layer is comprised of

oxide, silicon oxide, HDP or FSG; and the first and second metal contacts are each comprised of W or Cu.

50. The structure of claim 46, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised $CoSi_x$; the first ILD layer is comprised of silicon oxide; the metal gate portion is comprised of tungsten; the second ILD layer is comprised silicon oxide; and the first and second metal contacts each being comprised of tungsten.

51. The structure of claim 46, wherein the gate electrode has a width of from about 500 to 5000Å and the metal gate portion has a width of from about 500 to 8000Å.

52. The structure of claim 46, wherein the gate electrode has a width of from about 1000 to 3500Å and the metal gate portion has a width of from about 1000 to 3000Å.

53. The structure of claim 46, wherein the gate electrode has a width of about 0.13μm and the metal gate portion has a width of from about 1800 to 2400Å.

54. The structure of claim 46, wherein the gate electrode has a height of from about 1000 to 3000Å; the silicide portion over the gate electrode has a thickness of from

about 270 to 330Å; the first ILD layer has a thickness of from about 1700 to 1900Å; and the metal gate portion has a thickness of from about 1800 to 2200Å.

55. The structure of claim 46, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of from about 290 to 310Å; the first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of from about 1900 to 2100Å.

56. The structure of claim 46, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of about 300Å; the first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of about 2000Å.

57. The structure of claim 46, wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain silicide portion.

58. The structure of claim 46, wherein the MOSFET includes a source $CoSi_x$ silicide portion over at least a portion of the source and a drain $CoSi_x$ silicide portion over

at least a portion of the drain; and wherein the second metal contact contacts the drain $CoSi_x$ silicide portion.

59. The structure of claim 46, wherein the first ILD layer is planarized.

60. The structure of claim 46, wherein the high f_{MAX} deep submicron MOSFET structure is positioned within an RF circuit.

61. The structure of claim 46, wherein the gate electrode has a gate oxide thereunder; the gate oxide having a thickness proximate the source and drain to significantly reduce the parasitic capacitance and increase the f_{max} of the high f_{MAX} deep submicron MOSFET structure.

62. A high f_{MAX} deep submicron MOSFET structure, comprising:

a substrate;

a MOSFET on the substrate; the MOSFET having a source and a drain and including a silicide portion over a gate electrode; the gate electrode having a width of from about 500 to 5000Å;

a first ILD layer over the substrate and the MOSFET wherein the silicide portion over the gate electrode is exposed;

a metal gate portion:

over the first ILD layer;

and over the silicide portion over the gate electrode;

the metal gate portion having a width of from about 500 to 8000Å;

a second ILD layer over the metal gate portion and the first ILD layer;

a first metal contact through the second ILD layer contacting the metal gate portion; and

a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high f_{MAX} deep submicron MOSFET structure;

whereby the width of the metal gate portion reduces R_g and increases the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

63. The structure of claim 62, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

under the first ILD layer.

64. The structure of claim 62, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

between the first ILD layer;

the dielectric layer being comprised of Si_3N_4 or SiON.

65. The structure of claim 62, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised of $CoSi_x$, $CoSi_2$ or $TiSi_2$; the first ILD layer is comprised of oxide, silicon oxide, USG or TEOS; the metal gate portion is comprised of W, Al, Cu, TiN or Au; the second ILD layer is comprised of oxide, silicon oxide, HDP or FSG; and the first and second metal contacts are each comprised of W or Cu.

66. The structure of claim 62, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised $CoSi_x$; the first ILD layer is comprised of silicon oxide; the metal gate portion is comprised of tungsten; the

second ILD layer is comprised silicon oxide; and the first and second metal contacts each being comprised of tungsten.

67. The structure of claim 62, wherein the gate electrode has a width of from about 1000 to 3500Å and the metal gate portion has a width of from about 1000 to 3000Å.

68. The structure of claim 62, wherein the gate electrode has a width of about 0.13μm and the metal gate portion has a width of from about 1800 to 2400Å.

69. The structure of claim 62, wherein the gate electrode has a height of from about 1000 to 3000Å; the silicide portion over the gate electrode has a thickness of from about 270 to 330Å; the first ILD layer has a thickness of from about 1700 to 1900Å; and the metal gate portion has a thickness of from about 1800 to 2200Å

70. The structure of claim 62, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of from about 290 to 310Å; the first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of from about 1900 to 2100Å.

71. The structure of claim 62, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion 30 over the gate electrode 18 has a thickness of

about 300Å; the first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of about 2000Å.

72. The structure of claim 62, wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain silicide portion.

73. The structure of claim 62, wherein the MOSFET includes a source $CoSi_x$ silicide portion over at least a portion of the source and a drain $CoSi_x$ silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain $CoSi_x$ silicide portion.

74. The structure of claim 62, wherein the high f_{MAX} deep submicron MOSFET structure is positioned within an RF circuit.

75. The structure of claim 62, wherein the gate electrode has a gate oxide thereunder; the gate oxide having a thickness proximate the source and drain to significantly reduce the parasitic capacitance and increase the f_{max} of the high f_{MAX} deep submicron MOSFET structure.

76. The structure of claim 62, wherein the first ILD layer is planarized.

77. A high f_{MAX} deep submicron MOSFET structure, comprising:

a substrate;

a MOSFET on the substrate; the MOSFET having a source and a drain and including a silicide portion over a gate electrode; the gate electrode having a gate oxide thereunder; the gate oxide having a thickness proximate the source and drain to significantly reduce the parasitic capacitance and increase the f_{max} of the high f_{MAX} deep submicron MOSFET structure;

a first ILD layer over the substrate and the MOSFET wherein the silicide portion over the gate electrode is exposed;

a metal gate portion:

over the first ILD layer; and

over the silicide portion over the gate electrode;

the metal gate portion having a width substantially greater than the width of the silicide portion over the gate electrode;

a second ILD layer over the metal gate portion and the first ILD layer;

a first metal contact through the second ILD layer contacting the metal gate portion; and

a second metal contact through the second and first ILD layers contacting the drain completing the formation of the high f_{MAX} deep submicron MOSFET structure;

whereby the width of the metal gate portion reduces R_g and increases the f_{MAX} of the high f_{MAX} deep submicron MOSFET structure.

78. The structure of claim 77, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

under the first ILD layer.

79. The structure of claim 77, including a dielectric layer:

over the substrate and MOSFET but not over the silicide portion over the gate electrode; and

between the first ILD layer;

the dielectric layer being comprised of Si_3N_4 or SiON.

80. The structure of claim 77, wherein the gate electrode is comprised polysilicon; the silicide portion over the gate electrode is comprised of $CoSi_x$, $CoSi_2$, or $TiSi_2$; the first ILD layer is comprised of oxide, silicon oxide, USG or TEOS; the metal gate portion is comprised of W, Al, Cu, TiN or Au; the second ILD layer is comprised of

oxide, silicon oxide, HDP or FSG; and the first and second metal contacts are each comprised of W or Cu.

81. The structure of claim 77, wherein the gate electrode is comprised of polysilicon; the silicide portion over the gate electrode is comprised of $CoSi_x$; the first ILD layer is comprised of silicon oxide; the metal gate portion is comprised of tungsten; the second ILD layer is comprised of silicon oxide; and the first and second metal contacts are each comprised of tungsten.

82. The structure of claim 77, wherein the gate electrode has a width of from about 500 to 5000Å and the metal gate portion has a width of from about 500 to 8000Å.

83. The structure of claim 77, wherein the gate electrode has a width of from about 1000 to 3500Å and the metal gate portion has a width of from about 1000 to 3000Å.

84. The structure of claim 77, wherein the gate electrode has a width of about 0.13μm and the metal gate portion has a width of from about 1800 to 2400Å.

85. The structure of claim 77, wherein the gate electrode has a height of from about 1000 to 3000Å; the silicide portion over the gate electrode has a thickness of from

about 270 to 330Å; the first ILD layer has a thickness of from about 1700 to 1900Å; and the metal gate portion has a thickness of from about 1800 to 2200Å.

86. The structure of claim 77, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of from about 290 to 310Å; the first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of from about 1900 to 2100Å.

87. The structure of claim 77, wherein the gate electrode has a height of from about 1500 to 2200Å; the silicide portion over the gate electrode has a thickness of about 300Å; the first ILD layer has a thickness of about 1800Å; and the metal gate portion has a thickness of about 2000Å.

88. The structure of claim 77, wherein the MOSFET includes a source silicide portion over at least a portion of the source and a drain silicide portion over at least a portion of the drain; and wherein the second metal contact contacts the drain silicide portion.

89. The structure of claim 77, wherein the MOSFET includes a source $CoSi_x$ silicide portion over at least a portion of the source and a drain $CoSi_x$ silicide portion over

at least a portion of the drain; and wherein the second metal contact contacts the drain $CoSi_x$ silicide portion.

90. The structure of claim 77, wherein the first ILD layer is planarized.

91. The structure of claim 77, wherein the high f_{MAX} deep submicron MOSFET structure is positioned within an RF circuit. --